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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,872	09/16/2003	Vladimir M. Stojanovic	57941.000025	1169

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EXAMINER	
ODOM, CURTIS B	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,872	STOJANOVIC ET AL.	
	Examiner	Art Unit	
	Curtis B. Odom	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-88,106-109,142-147 and 172-175* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-71,142-147 and 172-175* is/are allowed.

6)☒ Claim(s) *72-74,76,80-88 and 106-109* is/are rejected.

7)☒ Claim(s) *75 and 77-79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 1-88, 106-109, 142-147, and 172-175 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 72-74, 76, 80-88, 106, and 107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (previously cited in Office Action 7/13/2006) in view of Thomas (U. S. Patent No. 3, 534, 273).

Regarding claim 72, Gitlin et al. discloses a method of operating a detector/non-linear canceller within an integrated circuit device (see Fig. 5,column 11, lines 48-50), the method comprising:

generating first and second decision (sample) values (Aj and Bj) using comparators (Fig. 4, blocks 431 and 432) of an input data signal (see column 6, line 64-column 7, line 5), each

value having either a first state (0) or a second state (1) according to whether the input data signal exceeds a respective one of first (V1) and second threshold levels (V2); and

generating a first received data value (current bit value) based on the first and second data (decision) values (see column 7, lines 8-16).

Gitlin does not disclose generating a second received data value (current bit) based on the first and second decision values if a mode select signal is in a certain state, wherein the second received data value includes more constituent bits than the first received data value.

However, Gitlin does disclose multi-level signaling could be applied to the above disclosed invention (see column 11, lines 14-22), wherein multi-level signaling would produce decision values with more constituent bits than binary signaling. Thomas further discloses two modes (binary and multi-level), wherein in a binary mode a single eye is used to determine the decision threshold levels and in a multi-level mode, multiple eyes are used to determine the decision threshold levels (see column 2, lines 60-71). Thomas further discloses three decision threshold are needed to detect a quaternary signal (see column 2, lines 28-35) of multiple constituent bits. Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since Gitlin discloses using multi-level signaling to modify the device of Gitlin to obtain decision thresholds for both a binary mode and multi-level mode as disclosed by Thomas in order to be able to implement both the binary and multi-level signaling and since Thomas states examining the eye allows optimum decision thresholds (see column 2, lines 60-71).

Regarding claim 73, Gitlin et al. further discloses operating the receiver using multi-level signaling (column 11, lines 14-21), wherein multi-level signaling includes signals with at least two bits.

Regarding claim 74, Gitlin et al. discloses creating a first received decision (data) value comprising one bit (see column 7, lines 8-16).

Regarding claim 76, Gitlin et al. further discloses generating a third data value (Fig. 5, Cj) having either the first state or the second state (0 or 1) according to whether the input data signal exceeds a third threshold level (V3).

Regarding claims 80 and 81, Giltin discloses generating the first and second samples by comparison comprises comparing the input signal in response to a first clock phase (transition), (see column 6, line 64-column 7, line 5 and column 12, lines 22-25).

Regarding claim 82, Gitlin et al. discloses generating the first received (bit) data value comprises selecting either the first data (decision) value or the second data value to be the received bit decision value (column 7, lines 8-16).

Regarding claim 83, Gitlin et al. discloses selecting either the first (decision) data value or the second data value to be the received (bit) data value (column 7, lines 8-16) comprises selecting either the first value or the second value according to whether a third sample (aj-1) is in the first state (0) or the second state (1).

Regarding claim 84, Gitlin et al. discloses the third data value (aj-1) is generated immediately prior to the first and second values (column 7, lines 8-16).

Regarding claim 85, Gitlin et al. discloses generating first and second thresholds (V1 and V2) using a reference signal generator (Fig. 4, block 438, column 6, lines 57-64).

Regarding claim 86, Thomas discloses two modes (binary and multi-level), wherein in a binary mode a single eye is used to determine the decision threshold levels and in a multi-level mode, multiple eyes are used to determine the decision threshold levels (see column 2, lines 60-71). Thomas further discloses three decision threshold are needed to detect a quaternary signal (see column 2, lines 28-35) of multiple constituent bits. Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since Gitlin discloses using multi-level signaling to modify the device of Gitlin to obtain decision thresholds for both a binary mode and multi-level mode as disclosed by Thomas in order to be able to implement both the binary and multi-level signaling and since Thomas states examining the eye allows optimum decision thresholds (see column 2, lines 60-71).

Regarding claim 87, Gitlin et al. further discloses the threshold levels are generated based upon the difference generated at subtracter 436 of Fig. 4 between signal levels (swings) of the input signals and the reference voltage levels (V1 and V2), see also column 5, lines 23-35).

Regarding claim 88, Gitlin et al. discloses generating threshold levels based on a rate of change of distortion (wherein intersymbol interference is distortion) in a channel (see column 5, lines 23-35).

Regarding claim 106, Gitlin et al. discloses detector/non-linear canceller which can be implemented as an integrated circuit device (Figs. 4 and 5, column 11, lines 48-50) comprising:

a first comparator (sampling) circuit (Fig. 4, block 411, column 6, line 64-column 7, line 10) to compare an input data signal with a threshold, the first comparator circuit being configured to generate a decision (sample) value having either a first state or a second state (0 or

1) according to whether the input data signal, when compared, is above or below a selected threshold level (V1); and

a reference signal generator (Fig. 4, block 438) representing a threshold generating circuit to establish the selected threshold level (column 6, lines 57-64) within the first comparator circuit, the threshold generating circuit establishing the selected threshold level at a first threshold level using a first operation mode involving a rate of change of distortion (column 5, lines 25-35) and establishing the selected threshold using a second mode of operation involving the use of an analog error signal (see column 11, lines 22-27).

Giltin does not disclose s threshold generating circuit to establish the selected threshold level within the first sampling circuit, the threshold generating circuit establishing the selected threshold level at a first threshold level if a mode select signal is in a first state, and establishing the selected threshold at a second threshold level if the mode select signal is in a second state.

However, Gitlin does disclose multi-level signaling could be applied to the above disclosed invention (see column 11, lines 14-22), wherein multi-level signaling would produce decision values with more constituent bits than binary signaling. Thomas further discloses two modes (binary and multi-level), wherein in a binary mode a single eye is used to determine the decision threshold levels and in a multi-level mode, multiple eyes are used to determine the decision threshold levels (see column 2, lines 60-71). Thomas further discloses three decision threshold are needed to detect a quaternary signal (see column 2, lines 28-35) of multiple constituent bits. Therefore, it would have been obvious to one skilled in the art at the time the invention was made that since Gitlin discloses using multi-level signaling to modify the device of Gitlin to obtain decision thresholds for both a binary mode and multi-level mode as disclosed

by Thomas in order to be able to implement both the binary and multi-level signaling and since Thomas states examining the eye allows optimum decision thresholds (see column 2, lines 60-71).

Regarding claim 107, Thomas discloses two modes (binary and multi-level), wherein in a binary mode a single eye is used to determine the decision threshold levels and in a multi-level mode, multiple eyes are used to determine the decision threshold levels (see column 2, lines 60-71). It would have been obvious to include this feature in order to be able to implement both the binary and multi-level signaling and since Thomas states examining the eye allows optimum decision thresholds (see column 2, lines 60-71).

4. Claims 108 and 109 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gitlin et al. (previously cited in Office Action 7/13/2006) in view of Thomas (U. S. Patent No. 3, 534, 273) as applied claim 106, and in further view of Popplewell et al. (previously cited in Office Action 7/13/2006).

Regarding claims 108 and 109, Gitlin and Thomas do not disclose a clock recovery circuit to generate a first clock signal that transitions at the time that corresponds to the transition interval within the input data signal, wherein the clock recovery circuit is coupled to receive the sample value generated by the first sampling circuit and is configured to advance or retard the phase of the first clock signal based, at least in part, on the state of the sample value.

However, Popplewell et al. discloses sampling an input signal at regular intervals and a threshold slicer which selects an ideal sample by comparing sampled values with received thresholds (see Abstract). Popplewell et al. further discloses further discloses a phase locked loop (Fig. 1) representing a clock recovery circuit to generate a first clock (oscillator) signal that

transitions (samples) on the frequency of interest of the input data signal (column 1, lines 28-36). Popplewell et al. also discloses a phase detector (Fig. 1, block 5) to receive a sample (column 3, lines 27-35) represented by a digital value and configured to align (advance or retard) the phase of the clock signal (Fig. 1, element 15, see column 1, lines 33-38) based on the phase error associated with the sample value which is used to phase align the clock signal using the oscillator (VFO) (see column 3, lines 31-43). Therefore, it would have been obvious to include modify the device of Gitlin and Thomas with this feature disclosed by Popplewell et al. since Popplewell et al. states correct alignment of the clock (oscillator) signal is critical in performing correct data recovery.

Allowable Subject Matter

5. Claims 1-40, 142-147, and 172-175 are allowable over prior art references because related reference do not disclose sampling data a third time to generate error samples. Claims 41 is allowable over prior art references because related reference do not disclose generating first and second voltage levels for sampling by subtracting a value representative of the first voltage level by a value representative of the second voltage level. Claims 42-52 are allowable over prior art references because related reference do not disclose controlling the samplers and storage circuits for the samplers using different clock signals. Claims 53-71 are allowable over prior art references because related references do not disclose comparing first and second samples to first and second thresholds, wherein in a first mode based on the comparison, outputting a most

significant bit and a least significant bit, and in a second mode of operation, based on the comparison, outputting the first sample or the second sample.

6. Claims 75 and 77-79 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wang et al. (U. S. Patent No. 5, 459, 762) discloses generating multiple sampling thresholds depending on the state of previous samples.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Curtis B. Odom whose telephone number is 571-272-3046. The examiner can normally be reached on Monday- Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Curtis Odom
January 5, 2007